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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/757,925	01/16/2004	Craig Hansen	43876-158	5116	
7590 04/19/2006			EXAMINER		
McDERMOTT, WILL & EMERY			TSAI, HENRY		
600 13th Street, N.W. Washington, DC 20005-3096			ART UNIT	PAPER NUMBER	
wasanigron, 2	20000 2020		2181		
			DATE MAILED: 04/19/2000	6	

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary		Applicati	plication No. Applicant(s)					
		10/757,9	25	HANSEN ET AL.				
		Examine	Т	Art Unit				
		Henry W.	H. Tsai	2181				
Period fo	The MAILING DATE of this communication Reply	ation appears on th	e cover sheet v	vith the correspondence a	ddress			
A SH WHIC - Exte after - If NC - Failu Any	ORTENED STATUTORY PERIOD FOR CHEVER IS LONGER, FROM THE MAIN IN IT IS LONGER IN IT IN IT IS LONGER IN IT IS LONGER IN IT IN IT IN IT IS LONGER IN IT IN IT IN IT IS LONGER IN IT IN I	LING DATE OF TI 37 CFR 1.136(a). In no evication. lory period will apply and w I, by statute, cause the app	HIS COMMUN rent, however, may a rill expire SIX (6) MO blication to become A	ICATION. I reply be timely filed INTHS from the mailing date of this of ABANDONED (35 U.S.C. § 133).				
Status								
1) 又	Responsive to communication(s) filed	on 18 June 2004		*				
2a)□)⊠ This action is r	on-final					
3)								
-/ت	closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.							
Disposit	ion of Claims	and an pant of	,,					
·		oliaation						
,	Claim(s) 1-39 is/are pending in the application.							
	4a) Of the above claim(s) is/are withdrawn from consideration.							
· <u> </u>	☐ Claim(s) is/are allowed.							
· —	Claim(s) 1-39 is/are rejected.							
7)∐	Claim(s) is/are objected to.	on and/or alastian r	oguirom ont					
8)□	Claim(s) are subject to restriction	on and/or election i	equirement.					
Applicat	ion Papers	•						
9)[The specification is objected to by the I	Examiner.						
10)🛛	10)⊠ The drawing(s) filed on <u>18 June 2004</u> is/are: a)⊠ accepted or b)□ objected to by the Examiner.							
	Applicant may not request that any objection	on to the drawing(s)	be held in abeya	ance. See 37 CFR 1.85(a).				
	Replacement drawing sheet(s) including the	ne correction is requir	red if the drawin	g(s) is objected to. See 37 C	FR 1.121(d).			
11)	The oath or declaration is objected to b	y the Examiner. N	ote the attache	ed Office Action or form P	TO-152.			
Priority (ınder 35 U.S.C. § 119							
a)	Acknowledgment is made of a claim for All b) Some * c) None of: 1. Certified copies of the priority do 2. Certified copies of the priority do 3. Copies of the certified copies of application from the International See the attached detailed Office action for the certification from the action for the attached detailed Office	ocuments have been been been the priority documents Bureau (PCT Ru	en received. en received in a ents have been le 17.2(a)).	Application No n received in this Nationa	l Stage			
Attachmen					•			
	e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (PTC)-Q48)		Summary (PTO-413) (s)/Mail Date				
3) 🔀 Infon	te of Draftsperson's Patent Drawing Review (PTC) mation Disclosure Statement(s) (PTO-1449 or PT r No(s)/Mail Date 2/1/06 6/10/05.			Informal Patent Application (PT	O-152)			

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 1-39 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims to computer-related inventions that are clearly nonstatutory fall into the same general categories as nonstatutory claims in other arts, namely natural phenomena such as magnetism, and abstract ideas or laws of nature which constitute "descriptive material. "Abstract ideas, Warmerdam, 33 F.3d at 1360, 31 USPQ2d at 1759, or the mere manipulation of abstract ideas, Schrader, 22 F.3d at 292-93, 30 USPQ2d at 1457-58, are not patentable. Descriptive material can be characterized as either "functional descriptive material" or "nonfunctional descriptive material." In this context, "functional descriptive material" consists of data structures and computer programs which impart functionality when employed as a computer component. (The definition of "data structure" is "a physical or logical relationship among data elements, designed to support specific data manipulation functions." The New IEEE Standard Dictionary of Electrical and Electronics Terms 308 (5th ed. 1993).) "Nonfunctional descriptive material" includes but is not limited to music, literary works and a compilation or mere arrangement of data (See MPEP section 2106, IV, B, 1).

Claim 1 comprises steps of decoding and providing. The steps are just an abstract idea. The claim do not provide practical application that produces a useful, tangible and

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concrete result. Therefore, the claim is non-statutory.

Similar problems exist in the other claims 2-11. As to claim

12, the additional step of multiplying is also an abstract idea.

The step does not make the claim statutory. Similar problems exist in claim 13.

In Claim 14, "a computer-redable medium" is not limited to statutory subject matter and is therefore non-statutory and note steps of decoding and providing are just an abstract idea. The claim do not provide practical application that produces a useful, tangible and concrete result. Similar problems exist in claim 26.

In claim 27, "a signal embodied in a transmission medium" is not limited to statutory subject matter and is therefore non-statutory since signals per se are not statutory and transmission medium can be non-statutory such as carrier wave. As set forth above, steps of decoding and providing are just an abstract idea. The claim does not provide practical application that produces a useful, tangible and concrete result. Similar problems exist in claim 39.

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Claim Objections

3. Claims 12, 25, and 38 are objected to because of the following informalities: In claim 12, line 5, "or" should read - of - . Similar problems exist in the other claims 25 and 38. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-10, 13-23, 26-36, and 39 are rejected under 35 U.S.C. 102(b) as being anticipated by Lahti (U.S. Patent No. 4,875,161), herein referred to as Lahti'161.

Referring to claim 1, Lahti'161 discloses, as claimed, a method of processing data in a programmable processor (the system comprising scientific processor 22, see Fig. 4), the method comprising: decoding a single instruction (see Fig. 20 A,

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regarding decoded instruction) for selectively arranging data, specifying a data selection operand (see Vector File address format in Fig. 13) and a first and a second register (block0 1350 and block1 1351 in Fig. 13 respectively) each having a register width, the first and second registers providing a plurality of data elements (such as words 0-63, se Fig. 13) each having an elemental width smaller than the register width, the data selection operand comprising a plurality of fields (see Col. 18, lines 30-50, regarding each field in Vector File address format) each selecting one (see Col. 18, lines 30-50, regarding an individual word is uniquely addressed) of the plurality of data elements; and for each field of the data selection operand, providing the data element (see col. 19, lines 7-63, regarding providing each word pair in each clock cycle) selected by the field to a predetermined position in a catenated result (such as Add Pipe Augend register 1318, see Fig. 13 or local store 168, see Fig. 4). Note claims 13, 14, 26, 27, and 29 recite the corresponding limitations as set forth in claim 1. As to Claims 26 and 39, Lahti'161 discloses the first register (block0 1350 in Fig. 13) providing a plurality of data elements (such as words 0, 1, 16, 17, 32, 33, 48 and 40, see Fig. 13).

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As to claim 2, Lahti'161 also discloses: the method of claim 1 wherein each field of the data selection operand provides a sufficient number of bits to specify any one of the plurality of data elements (see Col. 18, lines 30-50, regarding an individual word is uniquely addressed). Note Claims 15, and 28, recite the corresponding limitations as set forth in claim 2.

As to claim 3, Lahti'161 also discloses: the method of claim 2 wherein each field of the data selection operand has a width of n bits, wherein the plurality of data elements comprises 2^n data elements (see col. 18, lines 51-52, regarding $2^6 = 64$ words are selected). Note Claims 16, and 29, recite the corresponding limitations as set forth in claim 3.

As to claim 4, Lahti'161 also discloses: the method of claim 1 wherein the data selection operand is provided by a register specified by the single instruction (the instruction for vector processing since Lahti'161's system is used for a vector processing). Note Claims 17, and 30, recite the corresponding limitations as set forth in claim 4.

As to claim 5, Lahti'161 also discloses: the method of claim 4 wherein the data selection operand (see Vector File address format in Fig. 13) has a width equal to the specified register width (the widths for word 0 and 1 in block 0, see Fig.

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13 since the word width is changeable). Note Claims 18, and 31, recite the corresponding limitations as set forth in claim 5.

As to claim 6, Lahti'161 also discloses: the method of claim 1 wherein the catenated result is provided to a register (such as Add Pipe Augend register 1318, see Fig. 13 or local store 168, see Fig. 4). Note Claims 19, and 32, recite the corresponding limitations as set forth in claim 6.

As to claim 7, Lahti'161 also discloses: the method of claim 1 wherein the plurality of data elements has a combined width (the width for words 0/1 in block 0, and the width words 2/3 in block 1, see Fig. 13) equal to the width of the first register plus the width of the second register (block 0, and block 1, see Fig. 13). Note Claims 20, and 33, recite the corresponding limitations as set forth in claim 7.

As to claim 8, Lahti'161 also discloses: the method of claim 1 wherein the instruction further specifies a data element width of the plurality of data elements (<u>such as words 0-63</u>, <u>see Fig. 13</u>). Note Claims 21, and 34, recite the corresponding limitations as set forth in claim 8.

As to claim 9, Lahti'161 also discloses: the method of claim 1 wherein each data element has a width of 8 bits (note each word can be 8 bits in length). Note Claims 22, and 35, recite the corresponding limitations as set forth in claim 9.

As to claim 10, Lahti'161 also discloses: the method of claim 1 wherein the catenated result has a width of 128 bits (note each word can be 8 bits in length, therefore, the catenated result has a width of 8x16=128 bits when all the first pass in each block is transferred to the catenated result, see col. 19, lines 7-63, regarding providing each word pair in each clock cycle). Note Claims 23, and 36, recite the corresponding limitations as set forth in claim 10.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hamstra et al. discloses a local store for a scientific vector processor which provides high speed access to scalar variables, parameters, temporary operands, and register save area contents of the system. Basically, the local store is a general purpose storage structure which provides access which is as fast as access to the general or vector registers of the vector processor. The cache bank and the selected normal bank when continuous read commands are occurred to the selected normal bank.

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Fosdick discloses a microcoded central processing unit (CPU) is used to emulate the macroinstructions of a target computer. Each macroinstruction emulated is divided into two phases, an operand derivation or classification phase and an instruction execution phase. A microcontroller is provided to control each of the two separate phases. The two microcontrollers operate in parallel and simultaneously in performing their respective operations.

Contact Information

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (571) 272-4176. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Fritz M. Fleming, can be reached on (571) 272-4145. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the TC central telephone number, 571-272-2100.

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8. In order to reduce pendency and avoid potential delays,
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Please identify the examiner and art unit at the top of your
cover sheet. Papers submitted via FAX into Group 2100 will be
promptly forward to the examiner.

HENRY W. H. TSAI

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PRIMARY EXAMINEP

April 16, 2006